B.E SEM-VII C-Scheme Summer 2025 ECS.

21/6/25

Time: 3 hours **Max. Marks: 80**

N.B. (1) Question No. 1 is compulsory.
(2) Attempt any three questions from remaining five questions.
(3) All questions carry equal marks.
(4) Assume suitable data, if required and state it clearly.

Q1. Attempt any four. 20

a. List advantages of SRAM & DRAM.

b. Realize Boolean function F= $\overline{XY + Z}$ by static CMOS and dynamic CMOS logic style.

c. Compare constant voltage scaling and constant field scaling.

d. Explain briefly about transfer characteristics of CMOS inverter.

e. Draw and explain barrel shifter in brief.

Q2. a) Design 4:1 Multiplexer using pass transistor logic and CMOS transmission logic. 20

b) Explain design strategy of 6T SRAM cell.

Q3. a) Consider a CMOS Inverter circuit with the following parameters. 20

Vdd = 3.3V, Vtn = 0.6V, Vtp = -0.7V, Kn = 200μA/V2, Kp=80 μA/V2

Calculate Noise Margin of the circuit.

b) Explain Pseudo NMOS logic with suitable example.

Q4 a) Explain the working of resistive load NMOS Inverter. Derive expression for critical voltages. 20

b) Draw stick diagram and layout for CMOS based 2 input NOR gate.

Q5.a) Draw and explain clocked SR Latch using static CMOS design style 20

b) Explain carry skip, carry select and carry save high speed adders.

Q6. a) Explain working of CLA and how the speed of the adder can be enhanced? 20

b) Write short note on short channel effects.

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